IN THE SPECIFICATION

Replace the paragraph beginning on Page 7, line 29, with the following amended paragraph:

With regard to both embodiments, the row address pulses applied to the row conductors and the data signals applied to the column conductors and supplied by peripheral drive circuits in generally conventional manner. FIG. 6 shows schematically a display device according to the invention and using pixels of the kind described above with reference to FIGS. 2 and 3. The pixels P, each comprising a plurality of sub pixels, are organised in rows and columns to form a display pixel array 30. Typically, there may be several hundred rows and columns of pixels. The pixels P in the same row share the same row conductor, 35, each row of pixels thus having four associated row conductors in the case of the above described examples, while the pixels P in the same column share the same column conductor, 38. The pixels are driven by peripheral drive circuitry comprising a row drive circuit 40 connected to the set of row conductors 35 and a column drive circuit ~~40~~ 42 connected to the set of column conductors 38, the row and column drive circuits being arranged to provide the required row address pulses and data signals to the row conductors and column conductor

associated with a pixel as described above. In a respective row address period the pixels in one row are all addressed at the same time, using common row address pulses applied to their associated sub-set of row conductors 35 and appropriate data signals applied to their respective column conductors 38. Each row of pixels is addressed in sequence in a respective row address period in a frame period and repetitively addressed in similar manner in successive frame periods. The operation of the row and column drive circuits 40 and 42 is controlled and synchronised by a timing and control circuit 45 to which is supplied a video signal VS containing video information from which the data signals required for the sub pixels are derived. The row drive circuit 40 comprises a digital shift register type circuit similar to conventional row drive circuits but suitably modified so as to provide in a row address period the necessary row address pulses to a sub-set of row conductors Row n-Row n+3 when addressing a row of pixels, as described previously with reference to FIG. 4 or 5. Likewise, although generally similar to conventional column drive circuits, column drive circuit 42 is appropriately modified to provide data signals to each column conductor 38 in the manner required for the previously described operation of the pixels. In addition, the row and column drive

circuits are selectively controllable by the timing and control unit 45 in response to a mode selection control signal MS applied thereto so as to switch the manner of operation of these circuits between that required for a low power mode of operation of the pixels and that required for a video mode of operation of the pixels as previously discussed. The kind of modifications necessary to the row and column drive circuits for these purposes will be apparent to the skilled person.